CLAIMS

What is claimed is:

1. A method for fabricating at least one conductive element for use with at least one semiconductor device component, comprising:

providing the at least one semiconductor device component;

defining a first layer of the at least one conductive element from substantially unconsolidated conductive material at least partially over said at least one semiconductor device component;

defining at least one additional layer of the at least one conductive structure from substantially unconsolidated conductive material at least partially superimposed over said first layer; and

permitting said substantially unconsolidated conductive material to at least partially consolidate.

2. The method of claim 1, wherein said providing comprises providing said at least one semiconductor device component comprises providing a substrate layer of a carrier substrate.

3. The method of claim 2, wherein said defining said first layer comprises defining said first layer to be substantially entirely carried by said substrate layer.

4. The method of claim 1, wherein said providing comprises providing at least two semiconductor device components.

5. The method of claim 4, wherein said defining said first layer comprises defining said first layer to electrically connect said at least two semiconductor device components.

6. The method of claim 4, wherein said providing said at least two semiconductor device components comprises providing a semiconductor die.

7. The method of claim 4, wherein said providing said at least two semiconductor device components comprises providing a lead frame.

8. The method of claim 4, wherein said providing said at least two semiconductor device components comprises providing a packaged semiconductor device.

9. The method of claim 1, wherein said defining said first layer and said defining said at least one additional layer comprise defining said first layer and said at least one additional layer from an at least partially liquified thermoplastic conductive elastomer.

10. The method of claim 1, wherein said defining said first layer and said defining said at least one additional layer comprise defining said first layer and said at least one additional layer from an at least partially uncured conductive photopolymer.

11. The method of claim 1, wherein said defining said first layer and said defining said at least one additional layer comprise defining said first layer and said at least one additional layer from metal.

12. The method of claim 1, wherein said permitting said substantially unconsolidated conductive material to at least partially consolidate comprises permitting said substantially unconsolidated conductive material to at least partially harden.

13. The method of claim 1, wherein said permitting said substantially unconsolidated conductive material to at least partially consolidate comprises selectively consolidating said substantially unconsolidated conductive material in selected regions of each of said first layer and said at least one additional layer.

14. The method of claim 13, wherein said permitting said substantially unconsolidated conductive material to at least partially consolidate comprises directing a laser beam onto said selected regions.

15. A method for bonding a conductive element to a contact of a semiconductor device component, comprising:

providing a semiconductor device component with at least one contact;

defining a first layer of at least one conductive element from a layer comprising substantially unconsolidated conductive material;

defining at least one other layer of said conductive element from at least one layer comprising substantially unconsolidated conductive material; and

permitting said conductive material to at least partially consolidate.

16. The method of claim 15, wherein said providing said semiconductor device component comprises providing a carrier substrate.

17. The method of claim 15, wherein said providing said semiconductor device component comprises providing a semiconductor die.

18. The method of claim 15, wherein said providing said semiconductor device component comprises providing a packaged semiconductor device.

19. The method of claim 15, wherein said defining said first layer and said defining said at least one other layer comprise defining said first layer and said at least one other layer from an at least partially liquified thermoplastic conductive elastomer.

20. The method of claim 15, wherein said defining said first layer and said defining said at least one other layer comprise defining said first layer and said at least one other layer from an at least partially uncured conductive photopolymer.

21. The method of claim 15, wherein said defining said first layer and said defining said at least one other layer comprise defining said first layer and said at least one other layer from metal.

22. The method of claim 1, wherein said permitting said conductive material to at least partially consolidate comprises permitting said conductive material to at least partially harden.

23. The method of claim 15, wherein said permitting said conductive material to at least partially consolidate comprises selectively consolidating said conductive material in selected regions of each of said first layer and said at least one other layer.

24. The method of claim 23, wherein said permitting said conductive material to at least partially consolidate comprises directing a laser beam onto said selected regions.

25. A method of connecting at least two semiconductor device components, comprising:

orienting said at least two semiconductor device components adjacent each other;

forming at least one layer comprising conductive material on surfaces of said at least two semiconductor device components; and

defining at least one corresponding layer of at least one conductive element extending between and disposed in communication with at least one first contact pad of a first of said at least two semiconductor device components and at least one second contact pad of a second of said at least two semiconductor device components from said at least one layer comprising conductive material.

26. The method of claim 25, wherein said orienting at least two semiconductor device components comprises orienting at least one semiconductor device relative to a carrier substrate.

27. The method of claim 25, wherein said orienting at least two semiconductor device components comprises orienting two semiconductor devices relative to one another.

28. The method of claim 27, wherein said orienting at least two semiconductor device components further comprises orienting said two semiconductor devices relative to a carrier substrate.

29. The method of claim 25, wherein said orienting at least two semiconductor device components comprises orienting a semiconductor die relative to a plurality of leads.

30. The method of claim 25, further comprising disposing at least another layer comprising conductive material over at least said at least one corresponding layer of said at least one conductive element.

31. The method of claim 25, wherein said forming said at least one layer comprising conductive material comprises forming at least one layer comprising a conductive elastomer.

32. The method of claim 25, wherein said forming said at least one layer comprising conductive material comprises forming at least one layer comprising metal.

33. The method of claim 25, wherein said forming and said defining comprise thermal stereolithography.

34. The method of claim 25, wherein said forming comprises forming said at least one layer from unconsolidated conductive material.

35. The method of claim 33, wherein said forming said at least one layer from unconsolidated conductive material comprises forming said at least one layer from a liquified thermoplastic conductive elastomer.

36. A method of fabricating a circuit board comprising:
providing at least a portion of a dielectric substrate; and
stereolithographically fabricating at least one conductive element on said at least a portion of said substrate.

37. The method of claim 36, wherein said providing at least said portion of said dielectric substrate comprises providing at least one stereolithographically fabricated substrate layer.

38. The method of claim 37, wherein said stereolithographically fabricating said at least one conductive element and stereolithographic fabrication of said at least one substrate layer are effected in situ.

39. The method of claim 36, wherein said stereolithographically fabricating comprises:
forming a first layer of said at least one conductive element from substantially unconsolidated conductive material;
forming at least one additional layer of said at least one conductive element from substantially unconsolidated conductive material; and
permitting said substantially unconsolidated conductive material to at least partially consolidate.

40. A method for fabricating a circuit board, comprising:
stereolithographically fabricating at least a portion of a substrate; and
forming at least one conductive element on said at least a portion of said substrate.

41. The method of claim 40, wherein said forming said at least one conductive element comprises stereolithographically fabricating said at least one conductive element.

42. The method of claim 41, wherein said stereolithographically fabricating and said forming are effected in situ.

43. The method of claim 40, wherein said stereolithographically fabricating comprises:

defining a first layer of said substrate from substantially unconsolidated dielectric material;

defining at least one additional layer of said substrate from substantially unconsolidated dielectric material, said at least one additional layer being at least partially superimposed over said first layer; and

permitting said substantially unconsolidated dielectric material to at least partially consolidate.

44. The method of claim 43, wherein said permitting comprises permitting said substantially unconsolidated dielectric material to at least partially harden.

45. The method of claim 43, wherein said permitting said substantially unconsolidated dielectric material to at least partially consolidate comprises selectively consolidating said substantially unconsolidated dielectric material in selected regions of each of said first layer and said at least one additional layer.

46. The method of claim 45, wherein said permitting said substantially unconsolidated dielectric material to at least partially consolidate comprises directing a laser beam onto said selected regions.

47. A conductive element at least partially formed on at least one semiconductor device component, comprising a plurality of superimposed, contiguous, mutually adhered layers of conductive material.

48. The conductive element of claim 47, wherein said conductive material comprises a thermoplastic conductive elastomer.

49. The conductive element of claim 47, wherein said conductive material comprises a metal.

50. The conductive element of claim 47, configured to be carried by a single semiconductor device component.

51. The conductive element of claim 47, configured to at least partially electrically connect two semiconductor device components.

52. A semiconductor device comprising:
a semiconductor device component, and
at least one conductive element carried by said substrate, said at least one conductive element including a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material.

53. The semiconductor device of claim 52, wherein said at least one conductive element is substantially entirely carried by said semiconductor device component.

54. The semiconductor device of claim 53, wherein said semiconductor device component comprises a layer of a carrier substrate.

55. The semiconductor device of claim 53, wherein said semiconductor device component comprises a dielectric layer disposed on an active surface of a semiconductor die.

56. The semiconductor device of claim 52, wherein said conductive material comprises a thermoplastic conductive elastomer.

57. The semiconductor device of claim 52, wherein said conductive material comprises a metal.

58. The semiconductor device of claim 52, wherein said at least one conductive element communicates with a contact of said semiconductor device component.

59. The semiconductor device of claim 58, wherein said semiconductor device component comprises a carrier substrate.

60. The semiconductor device of claim 58, wherein said semiconductor device component comprises a semiconductor die.

61. The semiconductor device of claim 58, wherein said semiconductor device component comprises a packaged semiconductor device.

62. The semiconductor device of claim 52, wherein said semiconductor device component comprises leads.

63. The semiconductor device of claim 62, wherein said at least one conductive element contacts one of said leads.

64. A semiconductor device assembly, comprising:

a carrier; and

at least one semiconductor die adjacent said carrier, said semiconductor die including bond pads; and

conductive elements electrically connecting contacts of said carrier to corresponding bond pads, each of said conductive elements including a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material.

65. The semiconductor device assembly of claim 64, wherein said carrier comprises a carrier substrate.

66. The semiconductor device assembly of claim 64, wherein said carrier comprises leads.

67. The semiconductor device assembly of claim 64, wherein said conductive material comprises a thermoplastic conductive elastomer.

68. The semiconductor device assembly of claim 64, wherein said conductive material comprises a metal.

69. A semiconductor device assembly, comprising:

a semiconductor device having a plurality of contacts; and

at least one other semiconductor device having another plurality of contacts; and

at least one conductive element connecting at least contact of said plurality of contacts with a corresponding contact of said another plurality of contacts, said at least one conductive element including a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material.

70. The semiconductor device assembly of claim 69, wherein said conductive material comprises a thermoplastic conductive elastomer.

71. The semiconductor device assembly of claim 69, wherein said conductive material comprises a metal.

72. The semiconductor device assembly of claim 69, further comprising a carrier to which said at least one semiconductor device and said at least one other semiconductor device are secured.

73. The semiconductor device assembly of claim 72, further comprising at least one other conductive element connecting at least one contact of at least one of said semiconductor devices to a contact of said carrier.

74. The semiconductor device assembly of claim 73, wherein said at least one other conductive element comprises a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material.

75. A semiconductor device assembly, comprising:
a first semiconductor device component including at least one contact pad;
a second semiconductor device component including at least one contact pad; and
at least one conductive element connecting said at least one contact pad of said first semiconductor device component to said at least one contact pad of said second semiconductor device component, said at least one conductive element comprising a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material.

76. The semiconductor device assembly of claim 75, wherein said conductive material comprises a conductive elastomer.

77. The semiconductor device assembly of claim 75, wherein said conductive material comprises a metal.

78. The semiconductor device assembly of claim 75, wherein at least one of said first and second semiconductor device components comprises a semiconductor die.

79. The semiconductor device assembly of claim 78, wherein said at least one of said first and second semiconductor device components comprises a packaged semiconductor die.

80. The semiconductor device assembly of claim 75, wherein each of said first semiconductor device component and said second semiconductor device component comprises at least one semiconductor die.

81. The semiconductor device assembly of claim 75, wherein at least one of said first and second semiconductor device components comprises a carrier substrate.

82. The semiconductor device assembly of claim 81, wherein said carrier substrate includes a support structure and at least one conductive element in communication with said at least one contact pad thereof.

83. The semiconductor device assembly of claim 82, wherein at least one of said at least one conductive element and said support structure comprises a plurality of superimposed, contiguous, mutually adhered layers of material.

84. The semiconductor device assembly of claim 75, wherein said at least one conductive element is located on a surface of each of said first and second semiconductor device components.

85. The semiconductor device assembly of claim 84, wherein said at least one conductive element extends across a peripheral edge of at least one of said first and second semiconductor device components.

86. The semiconductor device assembly of claim 80, further comprising a carrier substrate upon which at least one of said semiconductor dice is disposed.

87. The semiconductor device assembly of claim 86, further comprising at least one other conductive element connecting at least one other contact pad of at least one of said semiconductor die to at least one contact pad of said carrier substrate.

88. The semiconductor device assembly of claim 87, wherein said at least one other conductive element comprises a plurality of superimposed, contiguous, mutually adhered layers of conductive material.

89. The semiconductor device assembly of claim 88, wherein said conductive material comprises a conductive elastomer.

90. The semiconductor device assembly of claim 88, wherein said conductive material comprises metal.

91. A circuit board, comprising:
a substrate including at least one layer of dielectric material; and
at least one conductive element comprising a plurality of superimposed, contiguous, mutually adhered layers of conductive material.

92. The circuit board of claim 91, wherein said substrate comprises a plurality of superimposed, contiguous, mutually adhered layers of dielectric material.

93. The circuit board of claim 91, wherein said at least one conductive element comprises a via that extends substantially vertically through said substrate.

94. The circuit board of claim 91, wherein said conductive material comprises a thermoplastic conductive elastomer.

95. The circuit board of claim 91, wherein said conductive material comprises a metal.

96. A flip-chip type semiconductor device, comprising:
a semiconductor die having bond pads on an active surface thereof; and
conductive elements connecting said bond pads to corresponding contact pads disposed in an area array over a surface of the flip-chip type semiconductor device, at least one of said conductive elements including a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material.

97. The flip-chip type semiconductor device of claim 96, further comprising a carrier on which said contact pads are disposed in said area array to which said conductive elements are connected.

98. The flip-chip type semiconductor device of claim 96, wherein said conductive elements extend laterally over said active surface of said semiconductor die.

99. The flip-chip type semiconductor device of claim 98, wherein said conductive elements are separated from said active surface by way of a dielectric layer.

100. The flip-chip type semiconductor device of claim 99, wherein said dielectric layer is stereolithographically fabricated.

101. The flip-chip type semiconductor device of claim 98, further comprising a protective covering over laterally extending portions of said conductive elements.

102. The flip-chip type semiconductor device of claim 101, wherein said contact pads are at least electrically exposed through said protective covering.

103. The flip-chip type semiconductor device of claim 101, wherein said protective covering is stereolithographically fabricated.

104. The flip-chip types semiconductor device of claim 96, further comprising conductive structures positioned on at least some of said contact pads.

105. The flip-chip type semiconductor device of claim 104, wherein at least one of said conductive structures includes a plurality of superimposed, contiguous, mutually adhered layers comprising conductive material.

106. A method for fabricating a conductive element, comprising:

placing at least one semiconductor device with a surface thereof in a horizontal plane;

recognizing a location and orientation of the surface of the at least one semiconductor device; and

stereolithographically fabricating a conductive element on the at least one semiconductor device, the conductive element comprising at least one layer of at least partially consolidated material.

107. The method of claim 106, further comprising storing data including at least one physical parameter of the at least one semiconductor device and of the conductive element in computer memory, and using the stored data in conjunction with a machine vision system to recognize the location and orientation of the at least one semiconductor device.

108. The method of claim 107, further comprising using the stored data, in conjunction with the machine vision system, to effect the stereolithographically fabricating.

109. The method of claim 106, further including securing the at least one semiconductor device to a carrier prior to placing the surface of the at least one semiconductor device in said horizontal plane.